CLAIMS

1. A programmable read only memory cell useful in a memory array having select and access lines, the memory cell comprising:

a MOS field effect transistor having a gate, a gate dielectric underlying the gate, and first and second doped semiconductor regions underlying both the gate dielectric and the gate in a spaced apart relationship to define a channel region therebetween;

a MOS data storage element having a conductive structure, an ultra-thin dielectric underlying the conductive structure, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, the first doped semiconductor region of the MOS data storage element being coupled to the first doped semiconductor region of the MOS field effect transistor;

a select line segment coupled to the gate of the MOS field effect transistor;

a first access line segment coupled to the second doped semiconductor region of the MOS field effect transistor; and

a second access line segment coupled to the conductive structure of the MOS data storage element.

2. The memory cell of Claim 1 wherein each of the MOS data storage elements comprises an inversion-enabled region underlying both the ultra-thin dielectric and the conductive structure and adjacent to the first doped region of the MOS data storage element.

3. The memory cell of Claim 1 wherein each of the MOS data storage elements comprises a second doped region underlying both the ultra-thin dielectric and the conductive structure and integrated with the first doped region of the MOS data storage element.

4. The memory cell of Claim 1 wherein the gate dielectric of the MOS field effect transistors and the ultra-thin dielectric of the MOS data storage elements are formed from a common layer of ultra-thin gate oxide.

5. The memory cell of Claim 1 wherein the gate dielectric of the MOS field effect transistors is thicker than the ultra-thin dielectric of the MOS data storage elements.

6. A programmable read only memory cell useful in a memory array having select and access lines, the memory cell comprising a select transistor coupled in series with a data storage element between two access lines, the select transistor further having a gate coupled to one of the select lines, and the data storage element comprising an ultra-thin dielectric for physical storage of data.

7. The memory cell of Claim 6 wherein the data storage element is a MOS half-transistor.

8. The memory cell of Claim 6 wherein the data storage element is a MOS capacitor.

9. A method of operating a programmable read only memory array comprising a plurality of row lines, a plurality of column lines, at least one source line, and a plurality of memory cells at respective crosspoints of the row lines and column lines, each of the memory cells comprising a MOS field effect transistor coupled in series with a MOS data storage element between one of the column lines and one of the at least one source line, the MOS transistor further having a gate coupled to one of the row lines and the MOS data storage element comprising an ultra-thin dielectric for physical storage of data, the method comprising:

applying a first voltage to a selected one of the row lines for turning on each of MOS field effect transistor having the gate thereof coupled to the selected row line;

applying a second voltage to a selected one of the column lines; and

applying a third voltage to the at least one source line;

wherein the second voltage and the third voltage cause a potential difference across the ultra-thin dielectric of the memory cell coupled to the selected row line and the selected column line that is sufficient to break down the ultra-thin dielectric thereof.

10. The method of Claim 9 wherein the breakdown of the ultra-thin dielectric is a hard breakdown.

11. The method of Claim 9 wherein the breakdown of the ultra-thin dielectric is a soft breakdown.

12. The method of Claim 9 wherein the first voltage is about 2.5 volts, the second voltage is about 7 volts, and the third voltage is about 0 volts.

13. The method of Claim 8 wherein the first voltage is about 7 volts, the second voltage is about 7 volts, and the third voltage is about 0 volts.

14. The method of Claim 8 wherein the first voltage is about 2.5 volts, the second voltage is about 2.5 volts, and the third voltage is about –4.5 volts.

15. A programmable read only memory array comprising a plurality of row lines, a plurality of column lines, at least one shared line, and a plurality of memory cells at respective crosspoints of the row lines and column lines in the memory, each of the memory cells comprising:

a MOS field effect transistor having a gate, a gate dielectric underlying the gate, and first and second doped semiconductor regions underlying both the gate dielectric and the gate in a spaced apart relationship to define a channel region therebetween; and

a MOS data storage element having a conductive structure, an ultra-thin dielectric underlying the conductive structure, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, the first doped semiconductor region of the MOS data storage element being coupled to the first doped semiconductor region of the MOS field effect transistor;

wherein one of the column lines is coupled to the second doped semiconductor region of the MOS field effect transistor or to the conductive structure of the MOS data storage element, and one of the at least one shared lines is coupled to the conductive structure of the MOS data storage element or to the second doped semiconductor region of the MOS field effect transistor.

16. The memory array of Claim 15 wherein each of the MOS data storage elements comprises an inversion-enabled region underling both the ultra-thin dielectric and the

conductive structure and adjacent to the first doped region of the MOS data storage element.

17. The memory array of Claim 15 wherein each of the MOS data storage elements comprises a second doped region underling both the ultra-thin dielectric and the conductive structure and integrated with the first doped region of the MOS data storage element.

18. The memory array of Claim 15 wherein the gate dielectric of the MOS field effect transistors and the ultra-thin dielectric of the MOS data storage elements are formed from a common layer of ultra-thin gate oxide.

19. A programmable read only memory array comprising a plurality of row lines, a plurality of column lines, at least one shared line, and a plurality of memory cells at respective crosspoints of the row lines and column lines in the memory, each of the memory cells comprising a select transistor coupled in series with a data storage element between one of the column lines and one of the at least one shared line, the select transistor further having a gate coupled to one of the row lines and the data storage element comprising an ultra-thin dielectric for physical storage of data.

20. The memory of Claim 19 wherein the data storage element is a MOS half-transistor.

21. The memory of Claim 19 wherein the data storage element is a MOS capacitor.

22. A non-volatile memory cell comprising a select transistor coupled in series with a data storage element, the data storage element comprising a conductive structure, an ultra-thin dielectric underlying said conductive for physical storage of data, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, said select transistor having a gate that is controllable to address said memory cell.

23. The memory cell of Claim 22 wherein the data storage element is a MOS half-transistor.

24. The memory cell of Claim 22 wherein the data storage element is a MOS capacitor.

25. The memory cell of Claim 22 wherein said ultra-thin dielectric is a gate oxide.

26. The memory cell of Claim 25 wherein said gate oxide is less than 50 angstroms thick.

27. The memory cell of Claim 25 wherein said memory cell is programmed by breaking down said gate oxide by applying a voltage between said conductive structure and said first doped semiconductor region.

28. The memory cell of Claim 27 wherein said memory cell is read by sensing a current through said data storage element during application of a voltage between said conductive structure and said first doped semiconductor region.

29. A MOS data storage element having a conductive structure, an ultra-thin dielectric underlying the conductive structure, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, said storage element being programmed by breaking down said ultra-thin dielectric and said storage element read by sensing a current through said storage element.

30. The memory cell of Claim 29 wherein said ultra-thin dielectric is a gate oxide.

31. The memory cell of Claim 30 wherein said gate oxide is less than 50 angstroms thick.